AMENDMENTS TO THE CLAIMS

Please amend Claims 1, 12, 31, and 40. Claims 2-6, 8-11, 13-20, 33, 37-39, and 42-44 remain as previously pending. Please add new Claims 50 and 51.

1. (Currently Amended) A method of searching a string of data for a match with a data string, the method comprising:

routing a series of assembly instructions to a processor having a first execution circuit for executing arithmetic and logic instructions, wherein the instructions can be performed out of an original program order as part of a predicted branch that has not yet been taken;

analyzing the series of assembly instructions to detect a search instruction to perform a search operation, the search instruction comprising a data string and a starting address for the search operation;

routing the search instruction undecoded to a data string manipulation circuit, independent of the first execution circuit, capable of performing string manipulation instructions;

routing the starting address for the search operation from the data string manipulation circuit to a cache memory array;

comparing portions of the data string with consecutive portions of data stored in the cache memory array;

generating a match signal for each portion of the data stored in the cache memory array that matches a respective compared portion of the data string;

identifying a plurality of match signals indicating the consecutive portions of the data stored in the cache memory array that together match the data string; and

routing an address of cached data matching the data string to the data string manipulation circuit, wherein the routing the address of cached data matching the data string is performed after any instructions are performed that modify data within the address.

2. (Previously Presented) The method of Claim 1, additionally comprising routing the data string from the data string manipulation circuit to the cache memory array.

3. (Previously Presented) The method of Claim 2, additionally comprising aligning the data string with the data stored in the cache memory array prior to said act of comparing.

4. (Previously Presented) The method of Claim 1, wherein said acts of identifying a plurality of match signals and routing an address of cached data is performed by a decoder.

5. (Previously Presented) The method of Claim 1, wherein the data string comprises a word.

6. (Previously Presented) The method of Claim 1, wherein the data string comprises a doubleword or a quadword.

7. (Cancelled)

8. (Original) The method of Claim 1, wherein said act of comparing is performed by a plurality of comparators.

9. (Original) The method of Claim 8, wherein the number of the plurality of comparators is equal to the number of bytes in a cache line of the cache memory array.

10. (Original) The method of Claim 1, wherein said act of comparing is performed with a plurality of subtractors.

11. (Original) The method of Claim 1, wherein said act of comparing is performed in one clock cycle.

12. (Currently Amended) A method of performing a cache search operation within a digital processing system, the method comprising:

routing a series of instructions to a processor having a general execution circuit for executing arithmetic and logic instructions, wherein the instructions can be performed out of an original program order as part of a predicted branch that has not yet been taken;

analyzing the series of instructions to detect a search instruction to perform a search operation, the search instruction comprising a starting address and a data string;

routing the search instruction to a data string manipulation circuit without intervention by the general execution circuit;

routing the starting address for the search operation from the data string manipulation circuit to a cache memory;

searching a cache line in the cache memory for data that matches the data string, wherein said cache line comprises more bytes than the data string; and

routing an address of cached data matching the data string to the data string manipulation circuit, wherein the routing the address of cached data matching the data string is performed after any instructions are performed that modify data within the address.

13. (Previously Presented) The method of Claim 12, additionally comprising aligning the data string with an offset of the starting address prior to said act of searching.

14. (Original) The method of Claim 12, wherein the data string manipulation circuit comprises a bus interface unit.

15. (Original) The method of Claim 12, wherein the data string manipulation circuit comprises a memory controller.

16. (Original) The method of Claim 12, wherein said act of routing an address of cached data is performed by a decoder.

17. (Original) The method of Claim 12, wherein said act of searching the cache line is performed by a plurality of subtractors.

18. (Original) The method of Claim 12, wherein said act of searching the cache line is performed by a plurality of comparators.

19. (Original) The method of Claim 18, wherein the number of comparators is equal to the number of bytes in the cache line.

20.   (Original) The method of Claim 12, wherein said act of searching a cache line is performed in a single cycle.

21. – 30. (Cancelled)

31.   (Currently Amended) A processor comprising:

a data memory comprising a plurality of cache lines, each cache line comprising a plurality of bytes of data;

an instruction fetch circuit;

a first instruction processing circuit coupled to the instruction fetch circuit and configured to perform arithmetic and logic instructions received from the instruction fetch circuit and wherein the processing circuit can process the arithmetic and logic instructions out of an original program order as part of a predicted branch that has not yet been taken;

a second instruction processing circuit coupled to the instruction fetch circuit and configured to perform data string operations such that data string instructions are issued after completion of arithmetic and logic instructions that modify data in associated source or destination address blocks of the data memory, the second instruction processing circuit being further configured to receive a data string and an instruction to perform a search operation beginning at a starting source or destination address of the data memory, the second instruction processing circuit further comprising:

a plurality of inputs coupled to the data memory such that each input is coupled to receive a different one of the plurality of bytes of data of the cache line, and

a plurality of comparators, each comparator coupled to a respective one of the plurality of inputs and configured to compare the byte of data of the cache line received by the respective input with a portion of the data string, each comparator further configured to generate a match signal when the byte of data matches the compared portion of the data string, the plurality of comparators further comprising a plurality of outputs; and

a decoder circuit coupled to the plurality of outputs to receive match signals from the plurality of comparators and configured to identify sequential portions of the cache line having data that, when combined, matches the data string.

32.   (Cancelled)

33.   (Previously Presented) The processor of Claim 31, wherein the number of comparators is equal to the number of bytes in the cache line.

34.–36. (Cancelled)

37.   (Previously Presented) The processor of Claim 31, wherein the entire cache line is compared to the data string in one bus cycle.

38.   (Original)   The processor of Claim 31, wherein the data memory comprises a Level 1 cache.

39.   (Previously Presented) The processor of Claim 31, wherein the second instruction processing circuit further comprises a memory controller.

40.   (Currently Amended) A cache memory circuit comprising:

a cache data memory means for holding at least one cache line comprising a plurality of bytes of data;

means for searching the at least one cache line for a data value, wherein said means for searching is coupled to said cache data memory means, and wherein said means for searching receives a starting address for a search operation of the at least one cache line and aligns the data value with an offset of the starting address to search multiple portions of the at least one cache line in one clock cycle for data that matches compared portions of the data value;

means for detecting a string of matches between the multiple portions of the at least one cache line and the compared portions of the data value;

means for performing arithmetic and logic operations including out of an original program order as part of a predicted branch that has not yet been taken; and

means for receiving a series of instructions, wherein said means for receiving is coupled to both said means for searching and said means for

performing, said means for receiving being further configured to forward a first instruction associated with the search operation to said means for searching and to forward second instructions associated with arithmetic and logic operations to said means for performing, wherein second instructions that modify data associated with the data value are performed before first instructions associated with the data value.

41. (Cancelled)

42. (Original) The cache memory circuit of Claim 40, wherein the means for searching comprises a plurality of subtractors.

43. (Original) The cache memory circuit of Claim 40, wherein the means for searching comprises a plurality of comparators.

44. (Original) The cache memory circuit of Claim 43, wherein the number of comparators is equal to the number of bytes in the cache line.

45.– 49. (Cancelled)

Please add the following new Claims.

50. (New) The method of Claim 1, wherein the comparing the portions of the data string comprises comparing an entire cache line in a single cycle.

51. (New) The cache memory circuit of Claim 40, wherein the means for searching searches an entire one of the at least one cache line in one clock cycle for data that matches compared portions of the data value.